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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,241	02/13/2002	Marko Karppanen	1154.41135X00	8874

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EXAMINER	
MCCARTHY, CHRISTOPHER S	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 05/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,241	KARPPANEN, MARKO	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *response to arguments*.

DETAILED ACTION

1. Claims 9-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Porterfield U.S. Patent 6,349,347, as cited in prior office action, which was mailed on 11/2/2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 9-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Porterfield U.S. Patent 6,349,347.

As per claim 9, Porterfield teaches a method for improving the reliability of a computer system including a bus, and at least one plug-in unit coupled thereto, comprising: providing to each of at least one plug-in unit a s separate interface circuit such that each said plug-in unit is connected to said bus via said interface circuit corresponding thereto (column 3, line 62 – column 4, line 27; column 1, lines 52-65); addressing a respective plug-in unit, via the bus, by addressing operations directed at said respective plug-in unit and which are monitored by interface circuit corresponding thereto (column 3, lines 30-33); performing a time duration operation of addressing of said plug-in unit; and checking the state of addressing of the addressed plug-in unit such that (i) when the addressing is ended before expiration of a

predetermined period of time, the time duration operation of addressing is terminated and a new time duration operation of addressing is set to commence at time of next occurrence of addressing, and (ii) when the duration operation of addressing exceeds the predetermined time period, the addressing to that plug-in unit is terminated by said interface circuit corresponding thereto by sending into the bus a signal indicating termination of addressing. (column 4, lines 54-61; column 3, lines 46-53).

As per claim 10, Porterfield teaches a method as defined in claim 9, wherein: the time duration of addressing is monitored using a watchdog timer with a predetermined timing set therein (column 4, lines 22-24).

As per claim 11, Porterfield teaches a method as defined in claim 9, wherein: when addressing is terminated an error signal is set by the interface circuit into an active state in the bus (column 4, lines 54-60).

As per claim 12, Porterfield teaches a method as defined in claim 9, wherein: when addressing is terminated an error signal indicating an error condition in the plug-in unit is set by the interface circuit into active state in the status register of the plug-in unit (column 4, lines 54-60).

As per claim 13, Porterfield teaches an interface circuit for providing local monitoring capability to a plug-in unit of a computer system including a bus; and at least one plug-in unit coupled to said bus; wherein a separate interface circuit is provided to connect each said plug-in unit to said bus and comprising: a watchdog timer (column 4, lines 22-25); first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto, and second means for sending into the bus a signal indication termination

of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer (column 4, lines 54-61; column 3, lines 46-53).

As per claim 14, Porterfield teaches an interface circuit as defined in claim 13, further comprising: means for setting an error signal into active state in the bus column 4, lines 54-61).

As per claim 15, Porterfield teaches an interface circuit as defined in 13, further comprising: for setting a signal indicating an error condition in the plug-in unit into an active state in the status register of the plug-in unit (column 4, lines 54-61).

As per claim 16, Porterfield teaches an interface circuit as defined in 14, further comprising: for setting a signal indicating an error condition in the plug-in unit into an active state in the status register of the plug-in unit (column 4, lines 54-61).

As per claim 17, Porterfield teaches an interface circuit as defined in 13, wherein: the bus is a CompactPCI bus (column 3, lines 13-16; column 2, lines 44-56). Porterfield teaches the utilization of the OnNow technology, which uses the protocols set forth by the ACPI specification, which teaches, in section 6.3, the hot-pluggability of a PCI bus. Therefore, since Porterfield teaches the inclusiveness of the ACPI protocol, it inherently teaches the use of a hot-pluggable PCI bus, which implies a basic function of a CompactPCI bus.

As per claim 18, Porterfield teaches an interface circuit as defined in claim 16, wherein the bus is a Compact PCI bus (column 3, lines 13-16; column 2, lines 44-56). Porterfield teaches the utilization of the OnNow technology, which uses the protocols set forth by the ACPI specification, which teaches, in section 6.3, the hot-pluggability of a PCI bus. Therefore, since

Porterfield teaches the inclusiveness of the ACPI protocol, it inherently teaches the use of a hot-pluggable PCI bus, which implies a basic function of a CompactPCI bus.

As per claim 19, Porterfield teaches an interface circuit as defined in claim 13, wherein each said interface circuit is provided as a part of said plug-in unit corresponding thereto (column 4, lines 10-27).

As per claim 20, Porterfield teaches a method according to claim 10, wherein: said watchdog timer is provided at each said interface circuit or at each said plug-in unit (column 4, lines 46-47).

As per claim 21, Porterfield teaches a computer system including a bus and at least one plug-in unit coupled thereto, wherein the improvement comprises: providing at least one interface circuit and at least one plug-in unit each of which is connected to said bus via a separate said interface circuit corresponding thereto, wherein each said interface circuit comprises a watchdog timer, first means for activating the watchdog timer upon start of an addressing operation directed to the plug-in unit corresponding thereto, and second means for sending into the bus a signal indicating termination of addressing, the termination of addressing being effected when the duration of said addressing exceeds a predetermined time duration for addressing, as measured by the watchdog timer (column 4, lines 10-61; column 3, lines 46-53).

As per claim 22, Porterfield teaches a computer system according to claim 21, wherein each said interface further comprises: means for setting an error signal into an active state in the bus (column 4, lines 54-60).

As per claim 23, Porterfield teaches a computer system according to claim 22, wherein each said interface circuit comprises means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit (column 4, lines 54-60).

As per claim 24, Porterfield teaches a computer system according to claim 23, wherein: the bus is a Compact PCI bus (column 3, lines 13-16; column 2, lines 44-56). Porterfield teaches the utilization of the OnNow technology, which uses the protocols set forth by the ACPI specification, which teaches, in section 6.3, the hot-pluggability of a PCI bus. Therefore, since Porterfield teaches the inclusiveness of the ACPI protocol, it inherently teaches the use of a hot-pluggable PCI bus, which implies a basic function of a CompactPCI bus.

As per claim 25, Porterfield teaches a computer system according to claim 21, wherein each said interface circuit comprises means for setting a signal indicating an error condition in the plug-in unit into an active state in a status register of the plug-in unit (column 4, lines 54-60).

As per claim 26, Porterfield teaches a computer system according to claim 21, wherein: the bus is a Compact PCI bus (column 3, lines 13-16; column 2, lines 44-56). Porterfield teaches the utilization of the OnNow technology, which uses the protocols set forth by the ACPI specification, which teaches, in section 6.3, the hot-pluggability of a PCI bus. Therefore, since Porterfield teaches the inclusiveness of the ACPI protocol, it inherently teaches the use of a hot-pluggable PCI bus, which implies a basic function of a CompactPCI bus.

As per claim 27, Porterfield teaches a computer system according to claim 21, wherein each said interface circuit is provided as a part of said plug-in unit corresponding thereto (column 4, lines 10-45).

As per claim 28, Porterfield teaches a computer system according to claim 27, wherein: the bus is a Compact PCI bus (column 3, lines 13-16; column 2, lines 44-56). Porterfield teaches the utilization of the OnNow technology, which uses the protocols set forth by the ACPI specification, which teaches, in section 6.3, the hot-pluggability of a PCI bus. Therefore, since Porterfield teaches the inclusiveness of the ACPI protocol, it inherently teaches the use of a hot-pluggable PCI bus, which implies a basic function of a CompactPCI bus.

Response to Arguments

3. Applicant's arguments filed 3/9/2005 have been fully considered but they are not persuasive.

The applicant argues that Porterfield does not teach wherein each plug-in device monitors itself as to the addressing function of the respective plug-in. The examiner respectfully disagrees. The applicant has argued that the compatibility bridge of Porterfield is the device that is in control of the configuration of the peer devices. The examiner concedes this notion; however, as the applicant has admitted in the remarks, Porterfield does teach wherein the actual bridge itself can be a peer device. Therefore, if the peer device is the PCI bridge and the bridge is the monitoring control of the respective peer device, then the respective peer device is monitoring itself. The applicant has argued that the bridge device of Porterfield also monitors other peer devices on the bus and argues that this is contradiction of the claimed present invention; however, the amended claims only cite "at least one plug-in unit". The applicant seems to contradict himself by saying each plug-in device must have its own interface circuit, but

then amends the claims to cite the "at least one of" language. The applicant is urged to change the "at least one of" language if indeed the invention is to comprise of more than one plug-in units; however, in light of the present claimed language, any change of language to comprise of the "more than one" language would be deemed as new scope.

In light of the above arguments, the rejected claims stand.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: see attached PTO-892.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
May 5, 2005